IN THE CLAIMS

1. (Cancelled).

2. (Previously Presented) The method of claim 3, said encapsulating further comprising filling said cavity with said molding material, wherein a surface of said semiconductor die is exposed to said strip.

3. (Currently Amended) A method of manufacturing an integrated circuit package, comprising:

providing a substrate comprising:

a first surface,

a second surface opposite said first surface,

a cavity through said substrate between said first and second surfaces, and

a conductive via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

applying a strip to said second surface of said substrate;

mounting a semiconductor die on said strip, at least a portion of said semiconductor die being disposed inside said cavity;

encapsulating in a molding material at least a portion of said first surface of said substrate;

removing said strip from said substrate; and

attaching a thermal element to an exposed surface of said semiconductor die, wherein said attaching comprises attaching said thermal element to said conductive via.

4. (Original) The method of claim 3, said attaching said thermal element comprising bonding a thermally conductive adhesive to said thermal element.

5. (Previously Presented) The method of claim 4, said attaching said thermal element further comprising attaching said thermally conductive adhesive to said second surface of said substrate.

6. (Previously Presented) The method of claim 3, said mounting said semiconductor die comprising disposing said die in its entirety inside said cavity.

7. (Previously Presented) The method of claim 3, said thermal element comprising a heat slug.

8. (Previously Presented) The method of claim 3, said substrate further comprising a multi-layer circuit trace.

9. (Previously Presented) The method of claim 3, further comprising, after said mounting said semiconductor die on said strip, interconnecting said semiconductor die to a first trace embedded in said first surface of said substrate.

10. (Original) The method of claim 9, said interconnecting comprising a thermo-sonic wire bonding process.

11. (Previously Presented) The method of claim 3, said encapsulating comprising a liquid molding process.

12. (Previously Presented) The method of claim 3, said encapsulating comprising a transfer molding process.

13. (Previously Presented) The method of claim 3, said encapsulating comprising encapsulating said first surface of said substrate substantially in its entirety.

14. (Previously Presented) The method of claim 3, further comprising attaching a solder element to a trace embedded in said first surface of said substrate.

15. (Previously Presented) The method of claim 3, said applying said strip comprising applying an adhesive material on at least a portion of said strip to said second surface of said substrate.

16. (Previously Presented) The method of claim 3, said strip comprising a high temperature stable polyimide.

17. (Original) The method of claim 15, said mounting said semiconductor die comprising attaching said semiconductor die to said adhesive material on said strip.

18. (Previously Presented) The method of claim 3, said applying said strip further comprising sealing at least a portion of said cavity.

19. (Currently Amended) A method of manufacturing an integrated circuit package, comprising:

providing a substrate comprising:

a first surface,

a second surface opposite said first surface,

a plurality of cavities, each said cavity through said substrate between said first and second surfaces, and

a plurality of conductive vias, each said via extending through said substrate and electrically connecting said first surface of said substrate with said second surface of said substrate;

applying a strip to said second surface of said substrate;

mounting a plurality of semiconductor dies on said strip, at least a portion of each said semiconductor die being disposed inside each said cavity;

encapsulating in a molding material at least a portion of said first surface of said substrate;

removing said strip from said substrate; and

for each of said plurality of semiconductor dies, attaching a thermal element to an exposed surface of each said semiconductor die, wherein said attaching comprises attaching said thermal element to at least one of said conductive vias.

20. (Original) The method of claim 19, further comprising singulating said substrate into a plurality of integrated circuit packages.

21. (Original) The method of claim 20, said singulating comprising a sawing process.

22. (Original) The method of claim 20, said singulating comprising a punching process.

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (Previously Presented) The method of claim 18, said applying said strip further comprising sealing an entire bottom portion of said cavity.

40. (Previously Presented) The method of claim 7, wherein said heat slug comprises copper.

41. (Previously Presented) The method of claim 3, wherein said integrated circuit package is a ball grid array integrated circuit package.

42. (Previously Presented) The method of claim 3, wherein said integrated circuit package is a land grid array integrated circuit package.

43. (Previously Presented) The method of claim 9, said interconnecting comprising a tape automated bonding process.

44. (Cancelled).

45. (Currently Amended) The method of claim [[44]] 3, said substrate comprising a trace electrically connected to said conductive via.

46. (Previously Presented) The method of claim 45, said trace having a ring-like shape around said cavity.

47. (Previously Presented) The method of claim 3, said integrated circuit package having a thickness dimension of about 1.0 mm.

48. (Previously Presented) The method of claim 47, said integrated circuit package having a width dimension of about 7 to 50 mm.

49. (Previously Presented) The method of claim 48, said integrated circuit package having a width dimension of about 35 mm.

50. (Previously Presented) The method of claim 4, said thermally conductive adhesive comprising an epoxy.

51. (Previously Presented) The method of claim 50, said thermally conductive adhesive comprising a silver-filled epoxy.

52. (Currently Amended) A method of manufacturing an integrated circuit package, comprising:

providing a substrate comprising:

a first surface,

a second surface opposite said first surface,

a cavity through said substrate between said first and second surfaces, and

a means for electrically connecting said first surface of said substrate with said second surface of said substrate;

applying, to said second surface of said substrate, a means for sealing at least a portion of said cavity;

mounting a semiconductor die on said means for sealing, at least a portion of said semiconductor die being disposed inside said cavity;

encapsulating in a molding material at least a portion of said first surface of said substrate;

removing said means for sealing from said substrate; and

attaching, to at least an exposed surface of said semiconductor die, a means for dissipating heat, wherein said attaching comprises attaching said means for dissipating heat to said means for electrically connecting said first surface of said substrate with said second surface of said substrate.

53. (Previously Presented) The method of claim 52, said encapsulating further comprising filling said cavity with said molding material, wherein a surface of said semiconductor die is exposed to said means for sealing.

54. (Previously Presented) The method of claim 52, said attaching said means for dissipating heat comprising bonding a thermally conductive adhesive to said means for dissipating heat.

55. (Previously Presented) The method of claim 54, said attaching said means for dissipating heat further comprising attaching said thermally conductive adhesive to said second surface of said substrate.

56. (Previously Presented) The method of claim 52, said mounting said semiconductor die comprising disposing said die in its entirety inside said cavity.

57. (Previously Presented) The method of claim 52, said substrate further comprising a multi-layer circuit trace.

58. (Previously Presented) The method of claim 52, said encapsulating comprising encapsulating said first surface of said substrate substantially in its entirety.

59. (Previously Presented) The method of claim 52, said attaching a means for dissipating heat further comprising attaching said means for dissipating heat to said means for electrically connecting said first surface of said substrate with said second surface.

60. (Previously Presented) The method of claim 52, said integrated circuit package having a thickness dimension of about 1.0 mm.

61. (Previously Presented) The method of claim 60, said integrated circuit package having a width dimension of about 7 to 50 mm.

62. (Previously Presented) The method of claim 61, said integrated circuit package having a width dimension of about 35 mm.

63. (New) The method of claim 19, said substrate comprising a trace electrically connected to said at least one conductive via.

64. (New) The method of claim 63, said trace having a ring-like shape around said cavity.

65. (New) The method of claim 52, said substrate comprising a trace electrically connected to said means for electrically connecting said first surface or said substrate with said second surface of said substrate.

66. (New) The method of claim 65, said trace having a ring-like shape around said cavity.